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| **Lecture 1 : Motivation of the Course** |
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| **1.1 Motivation of the course** |
| Why do some circuits work the first time and some circuits take over a year and multiple design iterations to work properly? Why can, for some circuits, the produced quantities easily be ramped up, and for others both circuit and process optimisation is needed. Why are some circuits running red-hot requiring expensive cooling solutions while other circuits , for similar performance, are running from small batteries in hand held gadgets? Why do some companies make money with successful innovations and why do some companies loose hundreds of millions of dollars of revenue just because they did not get their product on market in time. |
| The answer to these questions is (a lack of) system engineering : analysis and design of a system's relevant electrical parameters. The deep submicron CMOS technologies have moved the bottleneck from device and gate level issues to interconnects and communication (metal wires) bottle necks, where we currently do not have any design automation. This course aims to provide a working knowledge of system electrical issues at chip level related to remove or live with these new bottle-necks (so that the disasters in design can be avoided with proper structures and performance budgeting ) . |

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| **1.2 Course Objectives** | |
|  | The course provides for final year undergraduates a solid and fundamental engineering view of digital system operation and how to design systematically well performing digital VLSI systems exceeding consistently, customer expectations and competitor fears. The aim is to teach the critical methods and circuit structures to identify the key 1 % of the circuitry on-chip which dominates the performance, reliability, manufacturability, and the cost of the VLSI circuit. With the current utilisation of the deep submicron CMOS technologies (0.25 micron and below design rules) the major design paradigm shift is associated with the fact that the interconnections (metal Al or Cu wires connecting gates) and the chip communication in general is the main design object instead of active transistors or logic gates. The main design issues defining the make-or-break point in each project is associated with power and signal distribution and bit/symbol communication between functional blocks on-chip and off-chip. In the course we provide a solid framework in understanding: |
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|  | - Scaling of technology and their impact on interconnects |
|  | - Interconnects as design objects |
|  | - Noise in digital systems and its impact on system operation |
|  | - Power distribution schemes for low noise |
|  | - Signal and signalling conventions for on-chip and off-chip communication |
|  | - Timing and synchronisation for fundamental operations and signalling |
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|  | The course objective is to provide the student with a solid understanding of the underlying mechanism and solution techniques to the above key design issues, so that the student, when working as industrial designer, is capable of identifying the key problem points and focus his creative attention and 90% of available resources to right issues for 1% of the circuitry and leave the remaining 99% of circuitry to computer automated tools or unqualified engineers. |

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| **Lecture 2 : System approach to VLSI Design** | | | |
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| **2.1 What is System?** | | | |
| **2.1.1 Definition of System** | | | |
| A *system* is something which gives an *output* when it is provided with an *input* (see figure 1). | | | |
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|  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/2.1.gif  Figure 1. ***A simple System*** | |  |
| **2.1.2 System-on-Chip(SoC)** | | | |
| As the name suggests, its basically means *shrinking the whole system onto a single chip*.The most important feature of the chip is that its functionality should be comparable to that of the original system. It improves quality, productivity and performance. | | | |
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|  |  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/2.2.gif  Figure 2. ***An SoC example*** |  |

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| **2.2 Design Abstraction levels** | | | | |
| Every system should be decomposed into *three*fundamental domains: | | | | |
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| 1. Behavioral Domain | | | | |
| 2. Structural Domain | | | | |
| 3. Physical Domain | | | | |
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| In every domain, there are diffirent layers or levels of hierarchy. The following Onion Diagram will give a better understanding of this - | | | | |
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|  | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/2.3.jpg | |  |
| Figure 3. ***Onion Diagram*** | | | | |
| We can design the system at various layers, which are called *design abstraction levels*: | | | | |
| 1. Architechture | | 2. Algorithm | 3. Modules (or Functions) |  |
| 4. Logic | 5. Switch | 6. Circuit | 7. Device |  |
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| In this course, we are only dealing with Logic, Switch and Circuit levels. | | | | |

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| **Representation examples** | | | |
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|  | ***Behavioral Representation*** |  | ***Structural Representation*** |
|  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/2.4.gif |  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/2.5.gif |
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| **2.3 Delay and Interconnect Issues in physical circuits** | | | |
| It must be noted that when the adder described (in the above structural Representation) is realized physically, the output may not arrive at the instant the input is given i.e. if the input is given at time ***t=0***, output can be obtained at time ***t=t1>0***, where values of***t1*** may range from picoseconds to milliseconds, but never zero. | | | |
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|  | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/2.6.gif |  |
|  | | Figure 4:***Delay in system output*** |  |
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| These delays may occur in the devices used to realize the system. However, today the major concern of designers are are the*interconnecting wires* which connect the various devices. They are the major bottleneck in the speed of the systems today. They occur due to parasitic resistances and capicitances present in the circuits designed. | | | |

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| |  | | --- | | **Lecture 3 : Introduction to MOSFET** | |  |  |  |  |  |  | | --- | --- | --- | --- | | **3.1 Basic MOSFET Structure** | | | | | In the introduction to a **system**, we got an overview of various levels of design, viz. Architectural level design, Program level design, Functional level design and Logic level design. However we can't understand the levels of design unless we are exposed to the basics of operation of the devices currently used to realize the logic circuits, viz., **MOSFET** (**M**etal **O**xide**S**emiconductor **F**ield **E**ffect **T**ransistor). So in this section, we'll study the basic structure of MOSFET. | | | | |  | | | | | The cross-sectional and top/bottom view of MOSFET are as in figures 3.11 and 3.12 given below : | | | | |  | | | | |  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.1.GIF | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.2.GIF |  | |  | Fig 3.11:***Cross-sectional view of MOSFET*** | Fig 3.12: ***Top/Bottom View of MOSFET*** |  | |  | | | | | An n-type MOSFET consists of a **source**and a **drain**, two highly conducting n-type semiconductor regions which are separated from the p-type substrate by reverse-biased p-n diodes. A metal or poly crystalline gate covers the region between the source and drain, but is isolated from the semiconductor by the **gate oxide**. | | | | |
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| |  |  |  |  |  | | --- | --- | --- | --- | --- | | **3.2 Types of MOSFET** | | | | | | MOSFETs are divided into two types viz. **p-MOSFET** and **n-MOSFET** depending upon its type of source and drain. | | | | | |  | | | | | |  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.3.jpg | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.4.jpg | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.5.JPG |  | |  | ***Fig. 3.21: p-MOSFET*** | ***Fig. 3.22: n-MOSFET*** | ***Fig. 3.23: c-MOSFET*** |  | |  | | | | | | The combination of a **n-MOSFET** and a **p-MOSFET** (as shown in figure 3.21) is called **cMOSFET** which is the mostly used as MOSFET transistor. | | | | | |
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| |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | **3.3 MOSFET I-V Modelling** | | | | | | | We are interested in finding the ***output***characteristics (http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.6.gif) and the ***transfer*** charcteristics (http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.7.gif) of the MOSFET. In other words, we can find out both if we can formulate a mathematical equation of the form : | | | | | | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.8.gif | | | | | | | Intutively, we can say that voltage level specifications and the material parameters cannot be altered by designers. So the only tools in the designer's hands with which he/she can improve the performance of the device are its ***dimensions, W***and***L***(shown in top view of MOSFET fig 2). In fact, the most important parameter in the device simulations is ratio of W and L. | | | | | | | The equations governing the **output**and**transfer**characteristics of an **n**-MOSFET and **p**-MOSFET are : | | | | | | |  | | | | | | |  |  | **p-MOSFET:** | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.9.gif | **Linear**  **Saturation** |  | |  |  | |  |  |  | |  |  | **n-MOSFET:** | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.10.gif | **Linear**  **Saturation** |  | |
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| The **output** characteristics plotted for few fixed values of http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.11.giffor **p**-MOSFET and **n**-MOSFET are shown next : | | | | | | | |
|  | | | | | | | |
|  |  | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.13.jpg | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.12.jpg | |  |
|  | |  | ***Fig 3.31: p-MOSFET*** | | ***Fig 3.32: n-MOSFET*** | |  |
|  | | | | | | | |
| The **transfer** characteristics of both **p**-MOSFET and **n**-MOSFET are plotted for a fixed value of http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.16.gifas shown next : | | | | | | | |
|  | | | | | | | |
|  |  |  |  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.15.jpg |  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.14.jpg |  |
|  | |  | ***Fig 3.33: p-MOSFET*** | | ***Fig 3.34: n- MOSFET*** | |  |
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| Note: From now onwards in the lectures, we will symbolize MOSFET by MOS. | | | | | | | |

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| **3.4 C-V Characteristics of a MOS Capacitor** | | | | |
| As we have seen earlier, there is an *oxide layer* below *Gate* terminal. Since oxide is a very good *insulator*, it contributes to an oxide capacitance in the circuit. Normally, the capacitance value of a capacitor doesn't change with values of voltage applied across its terminals. However, this is not the case with *MOS capacitor*. We find that the capacitance of MOS capacitor changes its value with the variation in Gate voltage. This is because application of gate voltage results in the band bending of silicon substrate and hence variation in charge concentration at **Si-SiO2** interface. Also we can see (from fig.3.42 ) that thehttp://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.17.gifcurve splits into two (reason will be explained later), after a certain voltage, depending upon the frequency (high or low) of AC voltage applied at the gate. This voltage is called the ***threshold voltage***(**Vth**) of MOS capacitor. | | | | |
|  | | | | |
|  |  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.18.jpg | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.19.jpg |  |
|  |  | ***Fig 3.41: Cross-section view of MOS Capacitor*** | ***Fig 3.42: http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.17.gif plot of MOS Capacitor*** |  |

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| |  | | --- | | **Lecture 4 : MOS Capacitor** | |  |  |  |  |  | | --- | --- | --- | | **4.1 MOS as Capacitor** | | | | Refering to fig. 4.1, we can see there is an *oxide layer* below the *Gate* terminal. Since oxide is a very good *insulator*, it contributes to an oxide capacitance in the circuit. | | | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.18.jpg |  | Normally, the capacitance value of a capacitor doesn't change with values of voltage applied across its terminals. However, this is not the case with *MOS capacitor*. We find that the capacitance of MOS capacitor changes its value with the variation in Gate voltage. This is because application of gate voltage results in band bending in silicon substrate and hence variation in charge concentration at**Si-SiO2** interface. | | ***Fig 4.1: Cross-section view of MOS Capacitor*** |  | | |
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| |  |  |  |  |  | | --- | --- | --- | --- | --- | | **4.2 Modes of operation** | | | | | | Depending upon the value of gate voltage applied, the MOS capacitor works in three modes : | | | | | |  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.2.1.jpg | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.2.2.jpg | |  | |  | ***Fig 4.2a: Accumulation mode (grey layer - strong hole concentration)*** |  | ***Fig 4.2b: Depletion Mode (light grey layer - depletion region)*** |  | |  | | | | | | **1. Accumulation:** In this mode, there is accumulation of holes (assuming n-MOSFET) at the Si-SiO2 interface. All the field lines emanating from the gate terminate on this layer giving an effective dielectric thickness as the oxide thickness (shown in Fig. 4.2a). In this mode, Vg <0 | | | | | | **2. Depletion:**As we move from negative to positive gate voltages the holes at the interface are repelled and pushed back into the bulk leaving a depleted layer. This layer counters the positive charge on the gate and keeps increasing till the gate voltage is below threshold voltage. As shown in Fig. 4.2b we see a larger effective dielectric length and hence a lower capacitance. | | | | | |  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.2.3.jpg | **3. Strong Inversion:**When Vg crosses threshold voltage, the increase in depletion region width stops and charge on layer is countered by mobile electrons at Si-SiO2 interface. This is called inversion because the mobile charges are opposite to the type of charges found in substrate. In this case the inversion layer is formed by the electrons. Field lines hence terminate on this layer thereby reducing the effective dielectric thickness as shown in Fig. 4.2c) | |  | |  | **Fig 4.2c: Strong Inversion mode (grey layer - strong electron concentration, light grey - depletion region)** |  |  |  | |

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| **4.3 Capacitace calculation of MOS Capacitor** | | | | | |
| In the last chapter, we gave you an introduction of MOS as capacitor. In this chapter, we will see how MOS works as a capacitor with derivation of some related equations. | | | | | |
|  | | | | | |
|  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.1.jpg | By Gauss's Law: | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.2.gif |  |  |
| Also by thermal equilibrium: | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.3.gif |  |
| where **p** and **n**are hole and electron concentrations of substrate and http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.4.gifis hole or electron concentration of the corresponding intrinsic seminconductor. | | |
| We see that if we keep makinghttp://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.11.gif more and more -ve, the charges **Qs** and**Qm**keep increasing. Thus, it is acting like a good parallel plate capacitor. Its capacitance can be given as- | | |
| ***Fig 4.3: Gate and Depeletion charge of MOS Capacitor*** |  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.5.gif |  |
| For +ve bias voltage on gate, increasinghttp://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.11.gif will increase **Qm** and **Qs.** | | | | | |

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| Using the depletion approximation, we can write depletion width http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.6.gifas a function of http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.7.gif as | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.8.gif |
| where http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.9.gif is the substrate acceptor density,http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.10.gif is dielectric constant of substrate and http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.7.gif is the surface potential at substrate. | | |
| The depletion region grows with increased voltage across the capacitor until strong inversion is reached. After that, further increase in the voltage results in inversion rather than more depletion. Thus the maximum depletion width is: | | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.11.gif | | |
| Also, | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.12.gif |  |
| Therfore at | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.13.gif |  |
| But by Gauss's law, electrons must compensate for increasing **Qs**. | |  |
| So, | | Qs |
| where charge **Qi** is due to electrons in the inversion layer. | | |
|  | | |
| Earlier due to low electric field, the electron-hole pairs formed below the oxide interface recombine. However, once the electric field increases, the electron-hole pairs formed are not able to recombine. So the free electron concentration increases. | | |
|  | By Kirchoff's law, http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.11.gif is given by: http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.15.gif |  |
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| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.16.gif | | |

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| **Lecture 5 : MOS Capacitor (Contd...)** |
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| **5.1 Threshold Voltage Calculation** |
| **Threshold voltage**is that gate voltage at which the surface band bending is twice http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/5.1.gif,Where |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/5.2.gif |
| We know that the depth of depletion region for http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.7.gifis between **0**and http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/5.3.gif and is given by, |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.8.gif |
| **Charge** in depletion region at http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/5.4.gifis given by http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/5.5.gifwhere |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.11.gif |
| Beyond threshold, the total charge**Q**D in the seminconductor has to balance the charge on gate electrode, **Qs** i.e. http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.14.gifwhere we define the charge in the inversion layer as a quantity which needs to be determined. |
| This leads to following expression for gate voltage- |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/5.6.gif |

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| **5.2 C-V Characteristics** |
| The low frequency and high frequency C-V characteristics curves of a MOS capacitor are shown in fig 5.2. |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/5.2.JPG |
| ***Fig 5.2 : Low & High Frequency C-V curves*** |
| The **low frequency** or quasi-static measurement maintains thermal equilibrium at all times. This capacitance is the ratio of the change in charge to the change in gate voltage, measured while the capacitor is in equilibrium. A typical measurement is performed with an electrometer, which measures the charge added per unit time as one slowly varies the applied gate voltage. |
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| The **high frequency** capacitance is obtained from a small-signal capacitance measurement at high frequency. The bias voltage on the gate is varied slowly to obtain the capacitance versus voltage. Under such conditions, one finds that the charge in the inversion layer does not change from the equilibrium value corresponding to the applied DC voltage. The high frequency capacitance therefore reflects only the charge variation in the depletion layer and the (rather small) movement of the inversion layer charge. |

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| **5.3 Oxide Charge Correction** | | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/5.10.gif | | |
| To keep the value of http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.19.gifwithin -1 Volt and +1 Volt, an n-channel device has high http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.9.gifdoping (similarly, p-channel device has high http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.22.gifdoping). | | |
| |  | | --- | | **Lecture 6: MOSFET I-V characteristics** | |  |   6.1 derivation of I-V relationship | | |
| In this section, the relation between http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.1.gif and http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.11.gifis discussed. We assume that gate-body voltage drop is more thanthreshold voltage http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/4.19.gif, so that mobile  electrons are created in the channel. This implies that the transistor is either in linear orsaturation region. | | |
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| Here we will derive some simple I-V characteristics of MOSFET, assuming that the device essentially acts as a variable resistor between source and drain, and only drift ohmic current needs to be calculated. Also note that the MOSFET is basically a two-dimensional device. The gate voltagehttp://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.11.gifproduces a field in the vertical (x) direction, which induces charge in the silicon, including charge in the inversion layer. The voltage http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/3.16.gifproduces a field in the lateral (y) direction, and current flows (predominantly) in the y-direction. Strictly speaking, we must solve the 2-D Poisson and continuity equations to evaluate the I-Vcharacteristics of the device. These are analytically intractable. We therefore resort to the gradual channel approximation described below. | | |
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| To find the current flowing in the MOS transistor, we need to know the charge in the inversion layer. This charge, Qn(y) (per sq. cm ) is a function of position along the channel, since the potential varies going from source to drain. We assume that Qn(y)can be found at any point y by solving the Poisson equation only in the x direction, that is treating the gate-oxide-silcon system in the channel region very much like a MOS capacitor. This is equivalent to assuming that vertical electric field Ex is much larger than the horizontal electric field Ey, so that the solution of the 1-dimensional Poisson equation is adequate. This gradual channel approximation (the voltage varies only gradually along the channel) is quite valid for long channel MOSFETs since Ey is small. For Qn(y) using charge control relation at location y we have : | | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.2.gif | | |
| Now we turn our attention to evaluate the resistance of the infinitesimal element of length dy along the channel(as shown in fig 6.21). Assuming that only drift current is present and hence applying Ohm's law, we get : | | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.3.jpg | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.4.gif | | | |
| Here we have l = d**y, http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.5.gif**and A=Wxi, wherexi=inversion layer thickness. | | | |
| Now using equation (6.22), We have : | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.6.gif | |  |
| ***Fig 6.21: Cross Sectional View of channel*** | Since http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.7.gifis varying along the transverse direction, we define http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.8.gifas : | | | |

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| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.9.gif |
| Now using http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.8.gifin eqn (6.23) and rearranging the terms,we will get : |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.10.gif |
| Neglecting recombination-regeneration which implies I**DS(y) =** I**DS**i.e. current constant throughtout the channel. |
| Integrating RHS of eqn (6.26) from **0** to V**DS**and LHS from**0 to L**, we will get |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.11.gif |
| Now substituting **Qn(y)** from eqn (6.21) in eqn (6.27), we will get : |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.12.gif |

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| Eqn (6.29) holds true forhttp://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.13.gif. | |
| The drain current first increases linearly with the applied drain-to-source voltage, but then reaches a maximum value. This occurs due to the formation of depletion region between *pinch-off* *point* and drain. This behaviour is known as ***drain saturation***which is observed for http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.14.gifas shown in figure below. | |
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| *http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.15.jpg* | The saturation current **IDSsat** is given by eqn (6.210), |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.16.gif |
| ***Fig 6.22: IDS-VDS graph*** |  |
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| **6.2 Channel length modulation and body bias effect** | |
| The observed current ***IDS***does not saturate, but has a small finite slope as shown in fig 6.31. This is attributed as **channel** | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.17.jpg | **length modulation**. This in MOSFET is caused by the increase in depletion layer width at the drain as the drain voltage is increased. This leads to a shorter channel length (reduced by http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.18.gif) and increased drain current. When the channel length of MOSFET is decreased and MOSFET is operated beyond channel pinch-off, the relative importance of pinch-off length http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.18.gifwith respect to physical length is increased. This effect can be included in saturation current as : |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.19.gif |
| Herehttp://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.20.gifis called channel length modulation coefficient. |
| ***Fig 6.31: Actual vs Ideal IDS-VDS graph*** |  |
| Till now we assumed that the body of MOSFET is to be grounded. We will now take effect of **body bias** into account i.e. body being applied a negative voltage in case of n-MOSFET. Application of ***VSB > 0***increases the potential build up across the semiconductor. Depletion region widens in order to compensate for the extra required field, which implies higher **VT**. Viewing it from the point of energy band diagram, a higher potential needs to be applied to the gate in order to bend the bands by the same ammount in order to create the same electron concentration in the channel. With the application to the body bias, it modulates to the threshold voltage governed by the threshold voltage governed by the following equations : | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.21.gif | |
| where http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/6.22.gifis known as the **body coefficient**. | |

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| **Lecture 7: Advanced Topics** |
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| **7.1 Motivation for Scaling** |
| The reduction of the dimensions of a MOSFET has been dramatic during the last three decades. Starting at a minimum feature length of 10 mm in 1970 the gate length was gradually reduced to 0.15 mm minimum feature size in 2000, resulting in a 13% reduction per year. Proper scaling of MOSFET however requires not only a size reduction of the gate length and width but also requires a reduction of all other dimensions including the gate/source and gate/drain alignment, the oxide thickness and the depletion layer widths. Scaling of the depletion layer widths also implies scaling of the substrate doping density. |
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| In short, we will study simplified guidelines for shrinking device dimensions to increase transistor density & operating frequency and reduction in power dissipation & gate delays. |
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| |  |  | | --- | --- | | **7.2 Types of Scaling** | | | Two types of scaling are common: | (i) constant field scaling and | |  | (ii) constant voltage scaling. | | ***Constant field scaling*** yields the largest reduction in the power-delay product of a single transistor. However, it requires a reduction in the power supply voltage as one decreases the minimum feature size. | | | ***Constant voltage scaling*** does not have this problem and is therefore the preferred scaling method since it provides voltage compatibility with older circuit technologies. The disadvantage of constant voltage scaling is that the electric field increases as the minimum feature length is reduced. This leads to velocity saturation, mobility degradation, increased leakage currents and lower breakdown voltages. | | | After scaling, the different Mosfet parameters will be converted as given by table below : | |  |  |  |  | | --- | --- | --- | | ***Before Scaling*** | ***After Constant Field Scaling*** | ***After Constant Voltage Scaling*** | | ***L*** | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.1.gif | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.1.gif | | ***W*** | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.2.gif | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.2.gif | | ***t*** | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.3.gif | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.3.gif | | ***x*i** | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.4.gif | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.4.gif | | ***V*DD** | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.5.gif | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.11.gif | | ***V*Th** | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.6.gif | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.12.gif | | ***N*a**or***N*d** | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.7.gif | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.13.gif | | ***C*ox** | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.8.gif | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.8.gif | | ***I*DS** | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.9.gif | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.14.gif | | ***P*D** | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.10.gif | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.15.gif | |

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| Where ***s***=scaling parameter of MOS |

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| **7.3 Short Channel Effect** |
| So far our discussion was based upon the assumptions that channel was long and wide enough, so that “edge” effects along the four sides was negligible, longitudinal field was negligible and electric field at every point was perpendicular to the surface. So we could perform one-dimensional analysis using gradual channel approximation. But in devices where channel is short longitudinal field will not be negligible compared to perpendicular field. So in that case one-dimensional analysis gives wrong results and we will have to perform dimensional analysis taking into account both longitudinal and vertical fields. (which is out of the scope this course) |
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| ***When is a channel called a short channel?***   (i) When junction (source/drain) length is of the order of channel length.   (ii) L is not much larger then the sum of the drain and source depletion width. |
| We have shown below the comparative graphs of  **I-V** characteristics for both long channel and short channel length MOSFETs. From graph, it can be clearly concluded that when the channel becomes short, the current in saturation region becomes linearly dependent on applied drain voltage rather than being square dependent. |
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| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.16.jpg |
| ***Figure 7.3: Comparison of ID vs VDS characteristics for long and short channel MOSFET devices*** |

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| |  |  |  | | --- | --- | --- | | **7.4 Velocity Saturation** | | | | As we were assuming longitudinal field to be very small in the channel, the magnitude of carrier velocity **|vd|** was proportional to **|Ex|**. But it has been observed that for high values of **|Ex|**carrier velocity tends to saturate. It is no more proportional to **|Ex|**. This lack of proportionality at high **|Ex|** values is known as velocity saturation. | | | |  |  | | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.18.GIFhttp://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/7.17.gif | | |  |  | | ***Figure 7.4 Velocity Saturation*** |  | | |
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| |  | | --- | | **Lecture 8: Short Channel Effects** | |  |   **8.1 Motivation** |
| As seen in the last lecture as channel length is reduced, departures from long channel behaviour may occur. These departures, which are called ***Short Channel Effects***, arise as results of a two-dimensional potential distribution and high electric fields in the channel region. |
| For a given channel doping concentration, as the channel length is reduced, the depletion layer widths of source and drain junctions become comparable to channel length. The potential distribution in the channel now depends on both the tranverse field ***E*x**(controlled by the gate voltage and back-surface bias) and the longitudinal field ***E*y**(controlled by the drain bias). In other words, the potential distribution becomes two dimensional, and the gradual channel approximation (i.e.***E*x*>>* *E*y**) is no longer valid. This two dimensional potential results in the degradation of the threshold behaviour, dependence of threshold voltage on the channel length & biasing voltages and failure of the current saturation due to punch through effect. |
| |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | |  |  | | --- | --- | | **8.2 Mobility Degradation** | | | Mobility is important because the current in MOSFET depends upon mobility of charge carriers(holes and electrons). | | | We can describe this mobility degradation by two effects : | | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/8.2.GIF | (i)**Lateral Field Effect:**In case of short channels, as the lateral field is increased, the channel mobility becomes field-dependent and eventually velocity saturation occurs (which was referred to in the previous lecture). This results in current saturation.. | | (ii) **Vertical Field Effect:** As the vertical electric field also increases on shrinking the channel lengths, it results in scattering of carriers near the surface. Hence the surface mobility reduces (Also explained by the mobility dependence equation given below). | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/8.1.gif | | Thus for short channels, we can see (in the figure 8.2) the mobility degradation which occurs due to velocity saturation and scattering of carriers. | | ***Figure 8.2: Mobilty degradation graph*** |  | | **8.3 Subthreshold Current** | | | An effect that is exacerbated by short channel designs is the subthreshold current which arises from the fact that some electrons are induced in the channel even before strong inversion is established. For the low electron concentration (typically of subthreshold regime), we expect diffusion current (propotional to carrier gradients) to dominate over drift currents (propotional to carrier concentrations). For very short channel lengths, such carrier diffusion from source to drain can make it impossible to turn off the device below threshold. The subthreshold current is made worse by the DIBL effect(will be explained in later sections) which increases the injection of electrons from the source. | | | | |
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| **8.4 Threshold Voltage variation with Channel Length** | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/8.3.jpg | In case of long channel MOSFETs, gate has control over the channel and supports most of the charge. As we go to short channel lengths as seen in the graph above, the threshold voltage begins to decrease as the charge in the depletion region is now supported by the drain and the source also. Thus the gate needs to support less charge in this region and as a result, ***V*T**falls down.This phenomenon is known as ***charge sharing effect.*** |
| Now since***I*DS**is propotional to (***V*GS -*V*T**), therefore as ***V*T**begins to fall in case of short channels, ***I*DS** starts increasing resulting in larger drain currents. Also when ***V*GS**is zero and the MOSFET is in the cut off mode, since ***V*T** is small, (***V*GS -*V*T**) will be a small negative value and will result in leakage current which further multplied by the drain voltage will result in leakage power. In case of long channel MOSFETs, ***V*T**is large enough and (***V*GS -*V*T**) is a comparatively larger negative value, in cut off mode leakage power is very small. |
| ***Figure 8.41: Dependence of VT on L for MOSFET*** |  |

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| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/8.4.jpg | | **Transit Time:**As seen in previous lecture, the short channel results in*velocity saturation* over part of the channel. So the argument used to derive the transit time for long channel MOSFET is no longer valid for short channel MOSFETs. We note that the transit time will be larger if electrons were moving at maximum speed all over the channel. Thus, | | |
|  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/8.5.gif | |
| Figure 8.42 shows that the transit time of a device operating in the 'flat' part of***IDS-VGS***characteristics curve which concludes that transit time cannot be decreased by increasing further ***VGS****.* | | |
| ***Figure 8.42: IDS Vs VGS for short cn*** | |  |  | |
| |  |  | | --- | --- | | **8.4 Threshold Voltage variation with Channel Length (contd...)** | | | **Quantum Mechanical Increase Effect:**Another effect of quantum mechanics that also increases with scaling, is a shift in the surface potential required for strong inversion. This effect arises from so called "energy quantization" of confined particles which preludes electrons and holes from existing at zero energy in the conduction or valence bands. It is a direct consequence of the coupled *Poisson-Schrodinger equation* solution. This surface potential shift manifests itself as an increase in |***V*T**| which for the long devices is given by - | | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/8.6.gif | | | Above equation tells that |***V*T**| increases as devices are scaled down. | | | **8.5 Drain Induced Barrier Lowering (DIBL)** | | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/8.7.jpg | The source and drain depletion regions can intrude into the channel even without bias, as these junctions are brought closer together in short channel devices. This effect is called charge sharing (as mentioned earlier) since the source and drain in effect take part of the channel charge, which would otherwise be controlled by the gate. As the drain depletion region continues to increase with the bias, it can actually interact with the source to channel junction and hence lowers the potential barrier. This problem is known as ***Drain Induced Barrier Lowering (DIBL)***. When the source junction barrier is reduced, electrons are easily injected into the channel and the gate voltage has no longer any control over the drain current. In DIBL case, http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/8.8.gif. | | For figure 8.5, we can observe that under extreme conditions of encroaching source and drain depletion regions, the two curves can meet. | | ***Figure 8.5: Surface potential graph with constant gate voltage (VDS and L are varied) .*** |  | | | |
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| **8.6 Drain Punch Through** |
| When the drain is at high enough voltage with respect to the source, the depletion region arround the drain may extend to the source, causing current to flow irrespective of gate voltage (i.e. even if gate voltage is zero). This is known as ***Drain Punch Through***condition and the punch through voltage ***V*PT**given by : |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/8.9.gif |
| So when channel length **L**decreases (i.e. short channel length case), *punch through voltage* rapidly decreases. |
| **8.7 Hot Carrier Effect** |
| Electric fields tend to be increased at smaller geometries, since device voltages are difficult to scale to arbitrarily small values. As a result, various hot carrier effects appear in short channel devices. The field in the reversed biased drain junction can lead to impact ionization and carrier multiplication. The resulting holes contribute to substrate current and some may move to the source, where they lower source barrier and result in electron injected from source into p-region. In fact n-p-n transistor can result within source channel drain configuration and prevent gate control of the current. |
| Another hot electron effect is the transport of the energetic electrons over (or tunneling through) the barrier into the oxide. Such electrons become trapped in the oxide, where they change the threshold voltage and I-V characteristics of the device. Hot electron effects can be reduced by reducing the doping in the source and drain regions, so that the junction fields are smaller. However lightly doped source and drain regions are incompatible with small geometry devices because of contact resistances and other similar problems. A compromise design of MOSFET, called *Lightly Doped Drain*(***LDD***), using two doping levels with heavy doping over most of the source and drain areas with light doping in a region adjecent to the channel. The LDD structure decreases the field between drain and channel regions, thereby reduces injection into the oxide, impact ionization and other hot electron effects. |

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| **8.8 Surface States and Interface Trapped Charge** |
| At Si-SiO2 interface, the lattice of bulk silicon and all the properties associated with its periodicity terminate. As a result, localized states with energy in the forbidden energy gap of silicon are introduced at or very near to the Si-SiO2 interface. Interface trapped charges are electrons or holes trapped in these states. The probability of occupation of a surface state by an electron or by a hole is determined by the surface state energy relative to the Fermi level. An electron in conduction band can contribute readily to electrical conduction current while an interface trapped electron does not, except hopping among the surface states. Thus by trapping electrons and holes, surface states can reduce conduction current in MOSFETs. |
| Surface states can also act as localized generation-recombination centers and lead to leakage currents. |
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| **8.9 Conclusion** |
| Because short channel effects complicate device operation and degrade device performance, these effects should be eliminated or minimized, so that a physical short channel device can preserve the electrical long channel behaviour. |

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| **Lecture 9 : Introduction to Fabrication Process** |
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| **9.1 Motivation** |
| In the previous module, we did a detailed study about the MOSFET. VLSI circuits are very complex circuits i.e we cannot make circuits by interconnecting few single MOSFET transistors. A VLSI circuit consists of millions to billions of transistors. For this purpose, we use ***Photolithography*** which is a method/technology to create the circuit patterns on a silicon wafer surface and the process is called ***Fabrication.*** |
| In this lecture, we will study in detail photolithography, how it is done and what sort of materials are used for this purpose. |

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| **9.2 Photolithography** | | |
| Photolithography is the method that sets the surface dimensions (horizontal) of various parts of devices and circuits. Its goal is two fold. *First goal* is to create in and on the wafer surface a pattern whose dimensions are as close to the device requirements as possible. This is known as ***resolution of images*** on the wafer and the pattern dimensions are known as***feature or image sizes*** of the circuit. *Second goal* is the correct placement called ***alignment***or***registration*** of the circuit patterns on the wafer. The entire circuit patterns must be correctly placed on the wafer surface because misaligned mask layers can cause the entire circuit to fail. | | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/9.1.jpg |  | In order to create patterns on the wafer, the required pattern is first formed in the *reticles*or*photomasks*. The pattern on reticle or mask is then transfered into a layer of *photoresist*. Photoresist is a light sensitive material similar to the coating on a regular photographic film. Exposure to light causes changes in its structure and properties. If the exposure to light causes photoresist to change from a soluble to insoluble one, it is known as ***negative acting***and the chemical change is called***polymerization.***Similarly, if exposure to light causes it change from relatively non-soluble to much more soluble, it is known as***positive acting***and the term describing it is called as***photosolubilisation.***The exposure radiation is generally *UV*and *E-beam.* Removing the soluble portions with chemical solvents called ***developers*** leaves a pattern on the photoresist depending upon the type of mask used. A mask whose pattern exists in the opaque regions is called ***clear field mask***. The pattern could also be coded in reverse, and such masks are known as ***dark field masks***. |
| ***Figure 9.1: Clear Field mask*** |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/9.2.jpg |  | The result obtained from the photomasking process from different combinations of mask and resist polarities is shown in the following table: |
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| photoresisttab |
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| ***Figure 9.2: Dark Field mask*** |  | |
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| The second transfer takes place from the photoresist layer into the wafer surface layer. The transfer occurs when etchants remove the portion of the wafer's top layer that is not covered by the photoresist. The chemistry of the photoresists is such that they do not dissolve in the chemical etching solutions; they are *etch resistant*; hence the name *photoresists*.The etchant generally used to remove silicon dioxide is hydrogen fluoride (**HF**). | | |
|  | | |
| photomasking | | |
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| The choice of mask and resist polarity is a function of the level of dimensional control and defect protection required to make the circuit work. For example, sharp lines are not obtainable with negative photoresists while etchants are difficult to handle with positive photoresists. | | |
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| After the pattern has been taken on resist, the thin layer needs to be etched. Etching process is used to etch into a specific layer the circuit pattern that has been defined during the photomasking process. For example, aluminium connections are obtained after etching of the aluminium layer. | | |
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| etching | | |

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| **9.3 Fabrication Process** |
| **Why polysilicon gate?** |
| The most significant aspect of using polysilicon as the gate electrode is its ability to be used as a further mask to allow precise definition of source and drain regions. This is achieved with minimum gate to source/drain overlap, which leads to lower overlap capacitances and improved circuit performance. |
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| **Procedure:** |
| A thick layer of oxide is grown on the wafer surface which is known as *field oxide (FOX)*. It is much thicker than the gate oxide. It acts as shield which protects the underlying substrate from impurities when other processes are being carried out on the wafer. Besides, it also aids in preventing conduction between unrelated transistor source/drains. In fact, the thick FOX can act as a gate oxide for a parasitic MOS transistor. The threshold voltage of this transistor is much higher than that of a regular transistor due to thick field oxide. The high threshold voltage is further ensured by introducing *channel-stop* diffusion underneath the field oxide, which raises the impurity concentration in the substrate in the areas where transistors are not required. |
|  |
| A window is opened in the field oxide corresponding to the area where the transistor is to be made. A thin highly controlled layer of oxide is deposited where active transistors are desired. This is called *gate oxide* or *thinox.* A thick layer of silicon dioxide is required elsewhere to isolate the individual transistors. |
|  |
| The thin gate oxide is etched to open windows for the source and drain diffusions. Ion implantation or diffusion is used for the doping. The former tends to produce shallower junctions which are compatible with fine dimension processes. As the diffusion process occurs in all directions, the deeper a diffusion is the more it spreads laterally. This lateral spread determines the overlap between gate and source/drain regions. |
|  |
| Next, a gate delineation mask is used to determine the gate area. There has to be minimum overlap between gate and source/drain regions. This is referred to as *self-aligned* process because source and drain do not extend under the gate. Polysilicon is then deposited over the oxide. |
|  |
| The complete structure is then covered with silicon dioxide and contact holes are etched using contact window mask down to the surface to be contacted. These allow metal to contact diffusion or polysilicon regions. |
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| Metallization is then applied to the surface using interconnect mask and selectively etched to produce circuit interconnections. |
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| As a final step, the wafer is passivated and openings to the bond pads are etched to allow for wire bonding. Passivation protects the silicon surface against the ingress of contaminants than can modify circuit behavior. |

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| **Lecture 10 : General Aspects of CMOS Technology** |
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| **10.1 Gate Material** | |
| Metals have several advantages when considered as gate electrodes. The use of metal gates would certainly eliminate the problems of dopant penetration through the dielectric and subsequent gate depletion. The use of metals with appropriate work functions for NMOS and PMOS devices would led to transistors with symetrical and tailored threshold voltages. Most refractory metals are good choices for this application primarily due to their high melting points, which allow them to be used at high temperatures necessary for source-drain implant activation. However thermodynamic stability of metal-dielectric interfaces at processing temperatures are major concerns which need to be addressed in addition to more subtle issues of electrical properties, flat band voltage (ultimately threshold voltages) stability and the charge trapping at the interface. The problem with using aluminium is that once deposited, it cannot be subjected to high temperature processes. Copper causes a lot of trap generation when used as a gate material. | |
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| **10.2 Parasitic Capacitances** | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/10.1.jpg | Though a lot of parasitic capacitances exist in a MOSFET as shown in figure 10.2, but those of prime concern to us are the gate to drain capacitance (***C*gd**) and gate to source capacitance (***C*gs**) because they are common to input and output nodes and gate multiplied by gain during circuit operation. Thus they increase the input capacitance drastically and decrease the charging rate. |
| ***Figure 10.2: Parasitic capacitances in MOSFET*** |  |

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| **10.3 Self-aligned Silicon Gate Technology** | | |
| When the metal is used as the gate material, then the source and drain are deposited before the gate and thus to align the | | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/10.2.jpg |  | gate, mask aligners are used and errors in aligning takes place. In case of polysilicon gate process, the exposed gate oxide(not covered by polysilicon) is etched away and the wafer is subjected to dopant-source or ion-implant which causes source-drain deposition and also these are formed in the regions not covered by polysilicon and thus source and drain donot extend under the gate. This is called self-aligning process. |
| ***Figure 10.3: Cross sectional view of MOSFET under Self-algining process*** |  |  |
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| **10.4 Channel Stopper** | | |
| It is used to prevent the channel formation in the subtrate below the field oxide. For example, for a p-substrate, the channel stopper implant would p+ which will increase the magnitude of threshold voltage. | | |
| Irregular surfaces can cause "step coverage problems" in which a conductor thins and can even break as it crosses a thick to thin oxide boundary. One of the methods used to remove these irregularities is to pre-etch the silicon in areas where the field oxide is to be grown by arround half the final required field oxide thickness. LOCOS (will explain it shortly) oxidation done after this gives the planner field oxide/gate oxide interface. | | |
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| **10.5 Polysilicon Deposition** | | |
| The sheet resistance of undoped polysilicon is 10^8 ohms/cm and it can be reduced to 30 ohm/cm by heavy doping. The advantage of using polysilicon as gate material is its use as further mask to allow precise definition of source and drain. The polysilicon resistance affects the input resistance of the transistor and thus should be small for improving the RC time constant. For this, higher doping concentration is used. | | |

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| **10.6 Oxide Growth** | |
| Oxide gro+wn on silicon may result in an uneven surface due to unequal thickness of oxide grown from same thickness of | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/10.3.jpg | silicon. Stress along the edge of an oxidized area (where silicon has been trenched prior to oxidation to produce a plainer surface) may produce severe damage in the silicon. To relieve this stress, the oxidation temperature must be sufficiently high to allow the stress in the oxide to relieved by viscous flow. In the LOCOS process, the transistor area is masked by ***SiO2/SiN***sandwich and the thick field oxide is then grown. The oxide grows in both the directions vertically and also laterally under the sandwich and results in an encroachment into the gate region called as *bird's beak.* |
| ***Figure 10.6: Formation of bird's beak in MOSFET*** |  |
| This reduces the active area of the transistor and specially the width. Some improvements in the LOCOS process produce*Bird's crest*which reduces the encroachments, but it is non-uniform. | |

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| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/10.4.jpg | The goal is to oxidize Si only locally, whenever a field oxide is needed. This is necessary for the following reasons:  -- Local oxide penetrates into the ***Si,***so the ***Si-SiO2***interface is lower than the source-drain regions to be made later. This could not be achieved with oxidizing all of the ***Si***and then etching of unwanted oxide.  -- For device performance reasons, this is highly beneficial, if not absolutely necessary. |
| **10.7 Active Mask or Isolation Mask(thin-ox)** |
| It describes the areas where thin oxides are needed to implement the transistor gates and allow implantations to form p/n type diffusions. A thin layer of ***SiO2***is grown and covered with ***SiN***and this is used as mask. The *bird's bead*must be taken into account while designing thin-ox. |
| ***Figure 10.62: Comparison of the LOCOS process with and without some sacrificial polysilicon*** |  |

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| **Lecture 11 : General Aspects of CMOS Technology (contd...)** |
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| **11. Why polysilicon prefered over aluminium as gate material?** | |
| Because- | |
| 1) **Penetration of silicon substrate**: If aluminium metal is deposited as gate, we can't increase the temperature beyond 500 degree celcius due to the fact that aluminium will then start penetrating the silicon substrate and act as p-type impurity. | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/11.1.JPG | 2) **Problem with non-self alignment**: In case of aluminium gate, we have to first create source and drain and then gate implant. We can't do the reverse because diffusion is a high temperature process. And this creates parasitic overlap input capacitances***C*gd** and ***C*gs**(figure 11.11).***C*gd**is more harmful because it is a feedback capacitance and hence it is reflected on the input magnified by (***k+1***) times (recall Miller's theorem), where ***k***is the gain. So if aluminum is used, the input capacitance increases unnecessarily which further increases the charging time of the input capacitance. Therefore output doesn't appear immediately. |
| ***Figure 11.11: Self-alignment is not possible in case of Al gate due to Cgd and Cgs*** |  |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/11.2.JPG | If poly-silicon is used instead, it is possible to first create gate and then source & drain implant, which eliminates the problem of overlap capacitances ***C*gd** and ***C*gs.**  Resistivity of poly-silicon is ***10^8 ohm/cm***. So we need to dope poly-silicon so that it resembles a metal like ***Al***and its resistance is reduced to 100 or 300 ohm (although its still greater than ***Al***). |
| ***Figure 11.12 Self-alignment possible in case of poly-silicon*** |  |
| Time for charging capacitance varies as negative exponential of ***(RC)^(-1)*** where ***R***and ***C***are resistance and capacitance of the device. As we know the resistance is directly propotional to the length, so poly-silicon length should be kept small so that the resistance is not large, otherwise the whole purpose of decreasing **C** (hence the time constant ***RC***) will be nullified. | |

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| |  |  | | --- | --- | | **11.2 Channel stopper Implant** | | | As we know millions of transistors are fabricated on a single chip. To seperate (insulate) these from each-other, we grow thick oxides (called *field oxide*s). So, at very high voltages, inversion may set in the region below the field oxide also, despite the large thickness of these oxides. | | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/11.3.jpg | To avoid this problem, we do an implant in this region before growing the field oxide layer so that threshold voltage for this region is much greater than that for the desired active transistor channel region. This implant layer is called ***channel stopper implant****. (as shown in figure 11.21)* | | ***Figure 11.21: channel stopper implant before field oxide region is grown (yellow color region)*** |  | |
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|  | |  |  | | --- | --- | | **11.3 Local Oxidation of Silicon (LOCOS)** | | |  | | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/11.7.jpg | During etching, anything irregular becomes more irregular. So we grow oxide fields 50% above and 50% below the wafer. This is called LOCal Oxidation of Silicon(LOCOS). | | ***Figure 11.31: Formation of LOCOS*** |  |  |  |  | | --- | --- | | **Creation of LOCOS:** | | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/11.6.jpg | *0.45 m*U of silicon, when oxidized, becomes 1 *m*U of ***SiO2*** because of change in density. When field oxides are grown, there is an encroachment of the oxide layer in the active transistor region below the gate oxide, because of the affinity of the ***SiO2*** gate oxide for oxygen. The resulting structure resembles a*bird's beak*(as shown in figure 11.32) . This affects the device performance. | | ***Figure 11.32: bird's beak*** |  | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/11.5.jpg | If we use ***Si3N4*** as the gate dielectric, it will not let oxygen pass through. But due to mismatch of the thermal coefficients of ***Si*** and ***Si3N4***, hence the resulting stress produces a non-planar structure called ***bird's crest***(as shown in figure 11.33) . | | ***Figure 11.33: bird's creast*** |  | | The thermal coefficients of***Si***and ***SiO2***match. So when ***Si3N4*** is used as the gate dielectric, we first grow a thin oxide layer underneath. The stress, which would otherwise be generated on the account of the difference in the thermal coefficients of***Si***and ***SiO2*** is now reduced. Since ***SiO2***is now there, bird's beak will be formed. | | |
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| **Lecture 12 : CMOS Fabrication Technologies** |
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| **12.2 Twin Well Technology** |
| Using twin well technology, we can optimise NMOS and PMOS transistors separately. This means that transistor parameters such as threshold voltage, body effect and the channel transconductance of both types of transistors can be tuned independenly. |
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| n+ or p+ substrate, with a lightly doped epitaxial layer on top, forms the starting material for this technology. The n-well and p-well are formed on this epitaxial layer which forms the actual substrate. The dopant concentrations can be carefully optimized to produce the desired device characterisitcs because two independent doping steps are performed to create the well regions. |
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| The conventional n-well CMOS process suffers from, among other effects, the problem of unbalanced drain parasitics since the doping density of the well region typically being about one order of magnitude higher than the substrate. This problem is absent in the twin-tub process. |

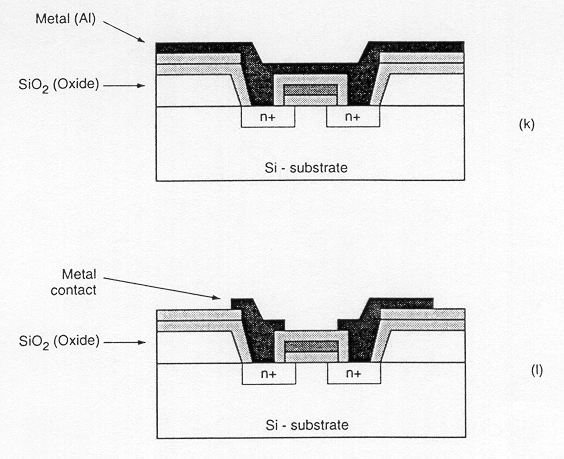
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| **12.3 Silicon on Insulator (SOI)** |
| To improve process characteristics such as speed and latch-up susceptibility, technologists have sought to use an insulating substrate instead of silicon as the substrate material. |
|  |
| Completely isolated NMOS and PMOS transistors can be created virtually side by side on an insulating substrate (eg. sapphire) by using the SOI CMOS technology. |
|  |
| This technology offers advantages in the form of higher integration density (because of the absence of well regions), complete avoidance of the latch-up problem, and lower parasitic capacitances compared to the conventional n-well or twin-tub CMOS processes. |
|  |
| But this technology comes with the disadvantage of higher cost than the standard n-well CMOS process. Yet the improvements of device performance and the absence of latch-up problems can justify its use, especially in deep submicron devices. |

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| |  | | --- | | **12.4 N-well Technology** | | In this discussion we will concentrate on the well established n-well CMOS fabrication technology, which requires that both n-channel and p-channel transistors be built on the same chip substrate. To accomodate this, special regions are created with a semiconductor type opposite to the substrate type. The regions thus formed are called wells or tubs. In an n-type substrate, we can create a p-well or alternatively, an n-well is created in a p-type substrate. We present here a simple n-well CMOS fabrication technology, in which the NMOS transistor is created in the p-type substrate, and the PMOS in the n-well, which is built-in into the p-type substrate. | |  | | Historically, fabrication started with p-well technology but now it has been completely shifted to n-well technology. The main reason for this is that, "n-well sheet resistance can be made lower than p-well sheet resistance" (electrons are more mobile than holes). | |  | | The simplified process sequence (shown in Figure 12.41) for the fabrication of CMOS integrated circuits on a p-type silicon substrate is as follows:   * N-well regions are created for PMOS transistors, by impurity implantation into the substrate * This is followed by the growth of a thick oxide in the regions surround the NMOS and PMOS active regions. * The thin gate oxide is subsequently grown on the surface through thermal oxidation. * After this n+ and p+ regions (source, drain and channel-stop implants) are created. * The metallization step (creation of metal interconnects) forms the final step in this process | | simpProcessSteps | | ***Fig 12.41: Simplified Process Sequence For Fabrication Of CMOS ICs*** | |  | | The integrated circuit may be viewed as a set of patterned layers of doped silicon, polysilicon, metal and insulating silicon dioxide, since each processing step requires that certain areas are defined on chip by appropriate masks. A layer is patterned before the next layer of material is applied on the chip. A process, called lithography, is used to transfer a pattern to a layer. This must be repeated for every layer, using a different mask, since each layer has its own distinct requirements. | |
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| **12.4 N-well Technology (contd.)** |
| We illustrate the fabrication steps involved in patterning silicon dioxide through optical lithography, using Figure 12.42 which shows the lithographic sequences. |
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| image |
| image |
| ***Fig 12.42: Process steps required for patterning of silicon dioxide*** |

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| **12.4 N-well Technology (contd.)** |
| First an oxide layer is created on the substrate with thermal oxidation of the silicon surface. This oxide surface is then covered with a layer of photoresist. Photoresist is a light-sensitive, acid-resistant organic polymer which is initially insoluble in the developing solution. On exposure to ultraviolet (UV) light, the exposed areas become soluble which can be etched away by etching solvents. Some areas on the surface are covered with a mask during exposure to selectively expose the photoresist. On exposure to UV light, the masked areas are shielded whereas those areas which are not shielded become soluble. |
|  |
| There are two types of photoresists, positive and negative photoresist. Positive photoresist is initially insoluble, but becomes soluble after exposure to UV light, where as negative photoresist is initially soluble but becomes insoluble (hardened) after exposure to UV light. The process sequence described uses positive photoresist. Negative photoresists are more sensitive to light, but their photolithographic resolution is not as high as that of the positive photoresists. Hence, the use of negative photoresists is less common in manufacturing high-density integrated circuits. |
|  |
| The unexposed portions of the photoresist can be removed by a solvent after the UV exposure step. The silicon dioxide regions not covered by the hardened photoresist is etched away by using a chemical solvent (HF acid) or dry etch (plasma etch) process. On completion of this step, we are left with an oxide window which reaches down to the silicon surface. Another solvent is used to strip away the remaining photoresist from the silicon dioxide surface. The patterned silicon dioxide feature is shown in Figure 12.43 |
|  |
| postlitho |
| ***Fig 12.43: The result of single photolithographic patterning sequence on silicon dioxide*** |
|  |
| The sequence of process steps illustrated in detail actually accomplishes a single pattern transfer onto the silicon dioxide surface. The fabrication of semiconductor devices requires several such pattern transfers to be performed on silicon dioxide, polysilicon, and metal. The basic patterning process used in all fabrication steps, however, is quite similar to the one described earlier. Also note that for accurate generation of high-density patterns required in submicron devices, electron beam (E-beam) lithography is used instead of optical lithography. |

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| |  | | --- | | **12.4 N-well Technology (contd.)** | | In this section, we will examine the main processing steps involved in fabrication of an n-channel MOS transistor on a p-type silicon substrate. | |  | | The first step of the process is the oxidation of the silicon substrate (Fig 12.44(a)), which creates a relatively thick silicon dioxide layer on the surface. This oxide layer is called field oxide (Fig. 12.44(b)). The field oxide is then selectively etched to expose the silicon surface on which the transistor will be created (Fig. 12.44(c)). After this the surface is covered with a thin, high-quality oxide layer. This oxide layer will form the gate oxide of the MOS transistor (Fig. 12.44(d)). Then a polysilicon layer is deposited on the thin oxide (Fig 12.44(e)). Polysilicon is used as both a gate electrode material for MOS transistors as well as an interconnect medium in silicon integrated circuits. The resistivity of polysilicon, which is usually high, is reduced by doping it with impurity atoms. | |  | | Deposition is followed by patterning and etching of polysilicon layer to form the interconnects and the MOS transistor gates (Fig. 12.44(f)). The thin gate oxide not masked by polysilicon is also etched away exposing the bare silicon surface. The drain and source junctions are to be formed (Fig 12.44(g)). Diffusion or ion implantation is used to dope the entire silicon surface with a high concentration of impurities (in this case donor atoms to produce n-type doping). Fig 12.44(h) shows two n-type regions (source and drain junctions) in the p-type substrate as doping penetrates the exposed areas of the silicon surface. The penetration of impurity doping into the polysilicon reduces its resistivity. The polysilicon gate is patterned before the doping and it precisely defines the location of the channel region and hence, the location of the source and drain regions. Hence this process is called a self-aligning process. | |  | | The entire surface is again covered with an insulating layer of silicon dioxide after the source and drain regions are completed (Fig 12.44(i)). Next contact windows for the source and drain are patterned into the oxide layer (Fig. 12.44(j)). Interconnects are formed by evaporating aluminium on the surface (Fig 12.44(k)), which is followed by patterning and etching of the metal layer (Fig 12.44(l)). A second or third layer of metallic interconnect can also be added after adding another oxide layer, cutting (via) holes, depositing and patterning the metal. |   image |
| image |
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| **12.4 N-well Technology (contd.)** |
| We now return to the generalized fabrication sequence of n-well CMOS integrated circuits. The following figures illustrate some of the important process steps of the fabrication of a CMOS inverter by a top view of the lithographic masks and a cross-sectional view of the relevant areas. |
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| The n-well CMOS process starts with a moderately doped (with impurity concentration typically less than 1015 cm-3) p-type silicon substrate. Then, an initial oxide layer is grown on the entire surface. The first lithographic mask defines the n-well region. Donor atoms, usually phosphorus, are implanted through this window in the oxide. Once the n-well is created, the active areas of the nMOS and pMOS transistors can be defined |
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| image |
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| The creation of the n-well region is followed by the growth of a thick field oxide in the areas surrounding the transistor active regions, and a thin gate oxide on top of the active regions. The two most important critical fabrication parameters are the thickness and quality of the gate oxide. These strongly affect the operational characteristics of the MOS transistor, as well as its long-term stability. |

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| **12.4 N-well Technology (contd.)** |
| Chemical vapor deposition (CVD) is used for deposition of polysilicon layer and patterned by dry (plasma) etching. The resulting polysilicon lines function as the gate electrodes of the nMOS and the pMOS transistors and their interconnects. The polysilicon gates also act as self-aligned masks for source and drain implantations. |
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| The n+ and p+ regions are implanted into the substrate and into the n-well using a set of two masks. Ohmic contacts to the substrate and to the n-well are also implanted in this process step. |
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| **12.4 N-well Technology (contd.)** |
| CVD is again used to deposit and insulating silicon dioxide layer over the entire wafer. After this the contacts are defined and etched away exposing the silicon or polysilicon contact windows. These contact windows are essential to complete the circuit interconnections using the metal layer, which is patterned in the next step. |
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| Metal (aluminum) is deposited over the entire chip surface using metal evaporation, and the metal lines are patterned through etching. Since the wafer surface is non-planar, the quality and the integrity of the metal lines created in this step are very critical and are ultimately essential for circuit reliability. |
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| The composite layout and the resulting cross-sectional view of the chip, showing one nMOS and one pMOS transistor (built-in n-well), the polysilicon and metal interconnections. The final step is to deposit the passivation layer (for protection) over the chip, except for wire-bonding pad areas. |
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| This completes the fabrication of the CMOS inverter using n-well technology. |
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| **Lecture 13 : Layout Design Rules** |
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| **13.1 Motivation** |
| In VLSI design, as processes become more and more complex, need for the designer to understand the intricacies of the fabrication process and interpret the relations between the different photo masks is really trouble some. Therefore, a set of layout rules, also called ***design rules***, has been defined. They act as an interface or communication link between the circuit designer and the process engineer during the manufacturing phase. The objective associated with layout rules is to obtain a circuit with optimum yield (functional circuits versus non-functional circuits) in as small as area possible without compromising reliability of the circuit. In addition, Design rules can be conservative or aggressive, depending on whether yield or performance is desired. Generally, they are a compromise between the two. Manufacturing processes have their inherent limitations in accuracy. So the need of design rules arises due to manufacturing problems like - |
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| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif Photo resist shrinkage, tearing.  http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif Variations in material deposition, temperature and oxide thickness.  http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif Impurities.  http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif Variations across a wafer. |
|  |
| These lead to various problems like : |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif*Transistor problems:*     Variations in threshold voltage: This may occur due to variations in      oxide thickness, ion-implantation and poly layer.      Changes in source/drain diffusion overlap.      Variations in substrate.  http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif*Wiring problems:*     Diffusion: There is variation in doping which results in variations in      resistance, capacitance.      Poly, metal: Variations in height, width resulting in variations in      resistance, capacitance.      Shorts and opens.  http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif *Oxideproblems:*       Variationsinheight.        Lack of planarity.  http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif *Via problems:*     Via maynot be cut all the way through.      Undersize via has too much resistance.      Via may be too large and create short. |
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| To reduce these problems, the design rules specify to the designer certain geometric constraints on the layout artwork so that the patterns on the processed wafers will preserve the topology and geometry of the designs. This consists of minimum-width and minimum-spacing constraints and requirements between objects on the same or different layers. Apart from following a definite set of rules, design rules also come by experience. |

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| **13.2 Types of Design Rules** |
| The design rules primary address two issues:  1. The geometrical reproduction of features that can be reproduced by the mask-  making and lithographical process ,and  2. The interaction between different layers. |
| There are primarily two approaches in describing the design rules. |
| **1. Scalable Design Rules (e.g. SCMOS, λ-based design rules) :** In this approach, all rules are defined in terms of a single parameter **λ**. The rules are so chosen that a design can be easily ported over a cross section of industrial process ,making the layout portable .Scaling can be easily done by simply changing the value of .  The key disadvantages of this approach are:  1. Linear scaling is possible only over a limited range of dimensions.  2. Scalable design rules are conservative .This results in over dimensioned and less dense design.  3. This rule is not used in real life. |
| **2. Absolute Design Rules (e.g. µ-based design rules ) :** In this approach, the design rules are expressed in absolute dimensions (e.g. 0.75µm) and therefore can exploit the features of a given process to a maximum degree. Here, scaling and porting is more demanding, and has to be performed either manually or using CAD tools .Also, these rules tend to be more complex especially for deep submicron. |
| The fundamental unity in the definition of a set of design rules is the minimum line width .It stands for the minimum mask dimension that can be safely transferred to the semiconductor material .Even for the same minimum dimension, design rules  tend to differ from company to company, and from process to process. Now, CAD tools allow designs to migrate between compatible processes. |

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| **13.3 Layer Representations** | | |
| With increase of complexity in the CMOS processes, the visualization of all the mask levels that are used in the actual fabrication process becomes inhibited. The layer concept translates these masks to a set of conceptual layout levels that are  easier to visualize by the circuit designer. From the designer's viewpoint, all CMOS designs have the following entities: | | |
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| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif Two different substrates and/or wells: which are p-type for NMOS and n-type for PMOS.  http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif Diffusion regions (p+ and n+): which defines the area where transistors can be formed. These regions are also called *active     areas*. Diffusion of an inverse type is needed to implement contacts to the well or to substrate. These are called *select     regions*.  http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif Transistor gate electrodes : Polysilicon layer  http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif Metal interconnect layers  http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif Interlayer contacts and via layers. | | |
|  | | |
| The layers for typical CMOS processes are represented in various figures in terms of: | | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif  A color scheme (Mead-Conway colors).  http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif  Other color schemes designed to      differentiate CMOS structures.  http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif  Varying stipple patterns  http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif  Varying line styles | | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/13.1.JPG |
|  | |
| An example of layer representations for CMOS inverter using above design rules is shown below- | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/13.2.jpg |  |
| ***Figure 13.32 :CMOS Inverter Layout*** | | ***Figure 13.31 Mead Conway Color coding for layers.*** |

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| **13.4 Stick Diagrams** |
| Another popular method of symbolic design is *"Sticks"* layout. In this, the designer draws a freehand sketch of a layout, using colored lines to represent the various process layers such as diffusion, metal and polysilicon .Where polysilicon crosses diffusion, transistors are created and where metal wires join diffusion or polysilicon, contacts are formed. |
| This notation indicates only the relative positioning of the various design components .The absolute coordinates of these elements are determined automatically by the editor using a compactor. The compactor translates the design rules into a set of constraints on the component positions ,and solve a constrained optimization problem that attempts to minimize the area or cost function. |
| The advantage of this symbolic approach is that the designer does not have to worry about design rules, because the compactor ensures that the final layout is physically correct. The disadvantage of the symbolic approach is that the outcome of the compaction phase is often unpredictable. The resulting layout can be less dense than what is obtained with the manual approach. In addition, it does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries. |
| For example, stick diagram for CMOS Inverter is shown below. |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/13.3.jpg |

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| **Lecture 14: λ-based Design Rules** |
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| 14.1 Background |
| As we studied in the last lecture, Layout rules are used to prepare the photo mask used in the fabrication of integrated circuits. The rules provide the necessary communication link between the circuit designer and process engineer. Design rules represent the best possible compromise between performance and yield. |
| The design rules primarily address two issues - |
| 1. The geometrical reproductions of features that can be reproduced by mask making and lithographical processes.  2. Interaction between different layers |
| Design rules can be specified by different approaches |
| 1. λ-based design rules 2. µ-based design rules |
| As λ-based layout design rules were originally devised to simplify the industry- standard µ-based design rules and to allow scaling capability for various processes. It must be emphasized, however, that most of the submicron CMOS process design rules do not lend themselves to straightforward linear scaling. The use of λ-based design rules must therefore be handled with caution in sub-micron geometries. |
| In further sections of this lecture, we will present a detailed study about λ-based design rules. |

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| **14.2 λ-based Design Rules** | | |
| **Features of λ-based Design Rules :**λ-based Design Rules have the following features- | | |
| * **λ** is the size of a minimum feature * All the dimensions are specified in integer multiple of **λ.** * Specifying **λ** particularizes the scalable rules. * Parasitic are generally not specified in **λ** units * These rules specify geometry of masks, which will provide reasonable yields | | |
| **Guidelines for using λ-based Design Rules:** | | |
|  | | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/14.1.JPG | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/14.2.JPG | |
| As, Minimum line width of poly is **2λ** & Minimum line width of diffusion is **2λ** | As Minimum distance between two diffusion layers **3λ** | |
|  | | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/14.3.JPG |  | As It is necessary for the poly to completely cross active, other wise the transistor that has been created crossing of diffusion and poly, will be shorted by diffused path of source and drain. |

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| **λ-based Design Rules (contd...)** | | |
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| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/14.4.JPG | ***Contact cut on metal*** | |
|  | |
| Contact window will be of **2λ** by **2λ** that is minimum feature size while metal deposition is of **4λ** by **4λ** for reliable contacts**.** | |
|  | | |
| ***In Metal*** |  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/14.5.JPG |
| Two metal wires have **3λ** distance between them to overcome capacitance coupling and high frequency coupling. Metal wires width can be as large as possible to decrease resistance. |
|  | | |
| http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/14.6.JPG | ***Buttering contact*** | |
|  | |
| Buttering contact is used to make poly and silicon contact. Window's original width is **4λ**, but on overlapping width is **2λ**. So actual contact area is **6λ** by **4λ**. | |

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| **λ-based Design Rules (contd...)** | | |
| The ***distance between two wells*** depends on the well potentials as shown above. The reason for 8l is that if both wells are at same high potential then the depletion region between them may touch each other causing punch-through. The reason for 6l is that if both wells are at different potentials then depletion region of one well will be smaller, so both depletion region will not touch each other so 6l will be good enough. |  | http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/Slides/images/14.7.JPG |
|  | | |
| The active region has length **10λ** which is distributed over the followings- | | |
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| **http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif 2λ** for source diffusion  http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif **2λ** for drain diffusion  **http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif 2λ** for channel length  **http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif 2λ** for source side encroachment  **http://www.cdeep.iitb.ac.in/nptel/Electrical%20&%20Comm%20Engg/VLSI%20Design/images/Bullet.gif 2λ** for drain side encroachment | | |

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|  | |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | | |  |  | | --- | --- | |  | **Module 4 : Propagation Delays in MOS** | |  | | |  | **Lecture 15 : CMOS Inverter Characteristics** | | | | |  | | | |  | | | |  | | | |  | | | |  |  | | |  |  | | |  | | | |  |  |  | |
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